IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 6. (Cancelled)

7. (Currently Amended) ~~The~~A memory device comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said floating gate with the interposition of an interpoly dielectric film, and

a peripheral circuit region having disposed therein a plurality of second MOS field effect transistors, each unitary transistor having a second well region formed in a semiconductor substrate, a second diffusion layer formed in said second well and designed to function as source and drain, and gate electrodes formed on said second well with the interposition of a gate insulating film,

wherein isolation between said plurality of second MOS field effect transistors is effected by a shallow groove isolation method, and at least one of said gate insulating films of said plurality of second MOS field effect transistors comprises a first deposited insulating film deposited on the semiconductor substrate,

wherein the interpoly dielectric film comprises a second deposited insulating film deposited on said floating gates which is substantially equal to said first

insulating film in thickness, wherein said second deposited insulating film is also deposited on said peripheral circuit region to comprise at least a portion of the gate insulating films of the second MOS field effect transistors,

wherein said first and second deposited insulating films are a silicon oxide films,

wherein nitrogen is introduced into said silicon oxide films, and

wherein the nitrogen concentration in said second deposited insulating film is higher than that in the first deposited insulating film.

8. – 13. (Cancelled)

14. (Currently Amended) ~~The~~A memory device comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said well with the interposition of an interpoly dielectric film, and

a peripheral circuit region provided with second MOS field effect transistors each having a second well region formed in the semiconductor substrate, a second diffusion layer formed in said second well region and designed to function as source and drain, and first gate electrodes formed on said second well with the interposition of a first gate insulating film, and third MOS field effect transistors each having a third well region formed in the semiconductor substrate, a third diffusion layer formed in

said third well region and designed to function as source and drain, and second gate electrodes formed on said third well with the interposition of a second gate insulating film which is greater than said first gate insulating film in thickness,

wherein isolation in said peripheral circuit region is effected by a shallow groove isolation method, and said second gate insulating film comprises a first deposited insulating film deposited on the semiconductor substrate,

wherein each of the interpoly dielectric film and the first gate insulating film comprises a second deposited insulating film, wherein a portion of the second deposited film forming the interpoly dielectric film is deposited on said floating gates and wherein said second deposited insulating film is also deposited in a position of the peripheral circuit region where said third MOS field effect transistors are formed to comprise at least a portion of the gate insulating films of the third MOS field effect transistors,

wherein both of the first and second deposited insulating films are a silicon oxide films,

wherein nitrogen is introduced into the silicon oxide films, and

wherein the nitrogen concentration in the films is higher in the order of the interpoly dielectric film, the first gate insulating film and the second gate insulating film.

15. – 42. (Cancelled)

43. (New) A memory device according to claim 7, wherein said gate insulating films of said second MOS field effect transistors are formed by depositing the second deposited of insulating film on the first deposited insulating film.

44. (New) A memory device according to claim 14, wherein said gate insulating films of said third MOS field effect transistors are formed by depositing the second deposited insulating film on said first deposited insulating film.

45. (New) A memory device comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said floating gate with the interposition of an interpoly dielectric film, and

a peripheral circuit region having disposed therein a plurality of second MOS field effect transistors, each unitary transistor having a second well region formed in a semiconductor substrate, a second diffusion layer formed in said second well and designed to function as source and drain, and gate electrodes formed on said second well with the interposition of a gate insulating film,

wherein isolation between said plurality of second MOS field effect transistors is effected by a shallow groove isolation method, and

means for preventing a kink in the current-voltage characteristics of the second MOS field effect transistors of the peripheral cell region, said means comprising forming a first layer of the gate insulating film of the second MOS transistors as a first deposited silicon oxide layer having nitrogen introduced therein, forming the interpoly dielectric film as a second deposited silicon oxide layer, having nitrogen introduced therein, on the floating gates in the memory cell region, and

forming a second layer of the gate insulating films of the second MOS field effect transistors as a portion of the second deposited silicon oxide film which is deposited on the first deposited silicon oxide film.

46. (New) A memory device according to claim 45, wherein the nitrogen concentration in the second deposited silicon oxide film is higher than that in the first deposited silicon oxide film.

47. (New) A memory device comprising:

a memory device comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said well with the interposition of an interpoly dielectric film, and

a peripheral circuit region provided with second MOS field effect transistors each having a second well region formed in the semiconductor substrate, a second diffusion layer formed in said second well region and designed to function as source and drain, and first gate electrodes formed on said second well with the interposition of a first gate insulating film, and third MOS field effect transistors each having a third well region formed in the semiconductor substrate, a third diffusion layer formed in said third well region and designed to function as source and drain, and second gate electrodes formed on said third well with the interposition of a second gate insulating

film which is greater than said first gate insulating film in thickness, wherein isolation in said peripheral circuit region is effected by a shallow groove isolation method, and

means for preventing a kink in the current-voltage characteristics of the third MOS field effect transistors of the peripheral cell region, said means comprising forming one layer of the gate insulating films of the third MOS field effect transistors as a first deposited silicon oxide film deposited on the substrate, said first deposited silicon oxide film having nitrogen introduced therein, forming the interpoly dielectric film as a second deposited silicon oxide film deposited on the floating gates in the memory cells region, and forming a second layer of the gate insulating film of the second MOS field effect transistors as a portion of the second deposited silicon oxide film which is deposited on the first deposited silicon oxide film.

48. (New) A memory device according to claim 47, wherein the nitrogen concentration in the silicon oxide films is higher in the order of the interpoly dielectric film, the first gate insulating film and the second gate insulating film.

49. (New) A memory device according to claim 14, wherein said third MOS field effect transistors have a higher breakdown voltage than the second MOS filed effect transistors.

50. (New) A memory device according to claim 47, wherein said third MOS field effect transistors have a higher breakdown voltage than the second MOS filed effect transistors.